86 GHz Static and 110 GHz Dynamic Frequency Dividers in SiGe Bipolar Technology

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Abstract **— We present static and dynamic frequency dividers manufactured in a 200 GHz f_T SiGe bipolar technology. The static divider has a divide ratio of 32 and operates up to 86.2 GHz. The dynamic divider is based on regenerative frequency division and has a divide ratio of two. It operates up to 110 GHz (limited by the measurement equipment). The power consumption of the static and dynamic frequency dividers is 900 mW and 310 mW, respectively.**

I. Introduction

Frequency dividers are used in a wide variety of applications and provide an important benchmark for the performance of high-speed technologies. Static frequency dividers using InP heterojunction bipolar transistors (HBTs) with maximum operating frequencies of 87 GHz [1] and 100 GHz [2] have been reported recently.

The fastest static frequency dividers in silicon germanium technology so far have achieved maximum operating frequencies of 71.8 GHz using conventional master-slave flip-flops [3] and 81 GHz using a pre-tracking technique [4].

The highest operating frequencies reported so far for dynamic dividers both in SiGe and III-V technologies are in the range of 90 GHz to 100 GHz. These dynamic frequency dividers are either based on clocked inverters [5] or on regenerative frequency division [6], [7], [8], [9].

In this paper we present a static and a dynamic frequency divider. Both circuits were designed to fully exploit the potential that advanced SiGe technologies offer for high-speed circuit design.

II. Circuit Design

A. Static Frequency Divider

The static frequency divider has a divide ratio of 32 and consists of five master-slave flip-flops (figure 1). The input signal is applied to the first divider stage via a pair of emitter followers. Figure 2 shows the schematic diagram of the first master-slave stage which determines the maximum operating frequency of the frequency divider. This stage uses two cascaded emitter followers to achieve the highest possible operating frequency. The current of the first emitter follower stage is used as reference current in the current mirror which determines the tail current of the latch. This enables a highly symmetric and very compact layout. The transistors in the latch operate at a current density of 7 mA/μm^2.

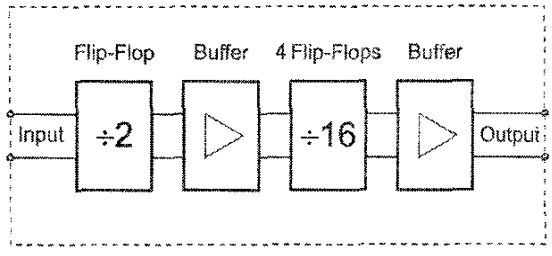

Fig. 1. Static frequency divider block diagram

The first flip-flop is followed by a buffer consisting of a differential amplifier and emitter followers. By using small transistors at the buffer input the capacitive load to the flip-flop is kept small, leading only to a slight decrease of the maximum operating frequency of the first divider stage. Emitter followers at the buffer output provide the clock signal for the four-stage asynchronous divider.

The flip-flops in these four divider stages are sim-

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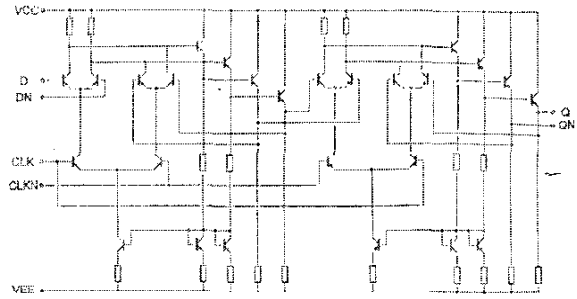

Fig. 2. Master-slave flip-flop

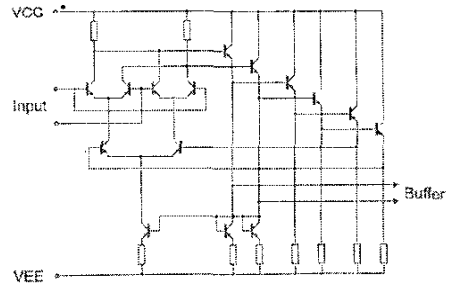

Fig. 4. Regenerative frequency divider using an active mixer

ilar to figure 2 but use only single emitter followers to reduce power consumption.

The last divider stage is followed by an output buffer which is designed to provide an output voltage swing of $> 2 \times 250\,\mathrm{mV}_{pp}$ at an external $50\,\Omega$ load.

B. Dynamic Frequency Divider

The dynamic frequency divider is based on the principle of regenerative frequency division. Figure 3 shows the block diagram. The input signal is applied to a mixer which is followed by a low-pass filter and an amplifier. The output signal is fed back to the second mixer input. When using an active mixer no separate amplifier is necessary. The frequency response of the mixer conversion gain shows low-pass behavior. Therefore no additional filter is required and the regenerative divider consists only of an active double-balanced mixer (figure 4). Three emitter follower stages are used in the feedback path of the mixer to obtain a high gain bandwidth. The output signal, which is then applied to a buffer amplifier, is taken from the first emitter follower stage. The two-stage buffer amplifier serves as limiter to make the output signal independent from the divider input amplitude.

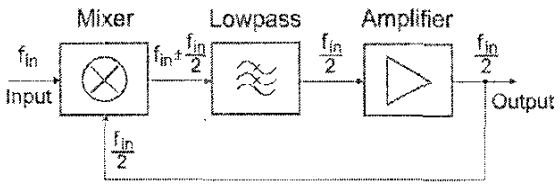

Fig. 3. Regenerative frequency division

III. Technology

The circuit is fabricated in an advanced SiGe bipolar process based on the technology presented in [7]. It uses a double-polysilicon self-aligned emitter-base configuration with effective emitter width of $0.15\,\mu\mathrm{m}$. The SiGe:C base is grown by selective epitaxy. The maximum transit frequency f_T of the transistors is 200 GHz. The technology provides three types of polysilicon resistors and four layers of metalization.

Fig. 5 shows a chip photograph of the static frequency divider. The chip size, which is determined by the pad frame, is $550\,\mu\mathrm{m}$ by $450\,\mu\mathrm{m}$.

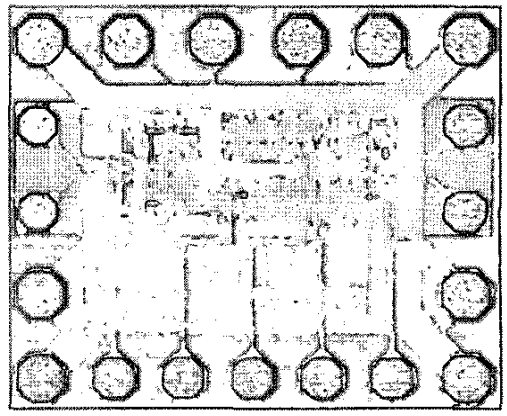

Fig. 5. Chip photograph of the static frequency divider (size: $550\ \mu\mathrm{m} \times 450\ \mu\mathrm{m}$)

IV. Measurement Results

A. Static Frequency Divider

Measurements were performed on wafer with a single-ended input signal. The complementary input was left unconnected.

Operating with a supply voltage of $-5\,\mathrm{V}$ the static frequency divider consumes 180 mA. Figure 6 shows the measured input sensitivity. The circuit operates up to a maximum input frequency of

86.2 GHz. The low-frequency response is limited by the slew-rate of the sinusoidal input signal.

Figure 7 shows the single-ended output signal of the frequency divider at an input frequency of 86.2 GHz. The output voltage swing is larger than $300\,\mathrm{mV}_{pp}$.

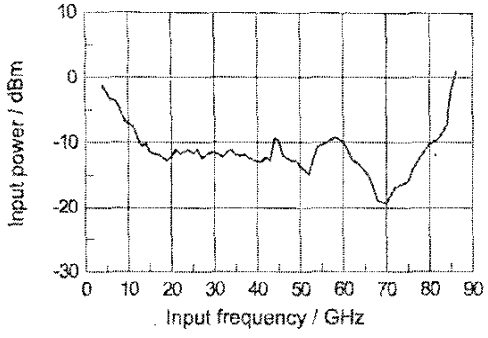

Fig. 6. Input sensitivity of the static frequency divider

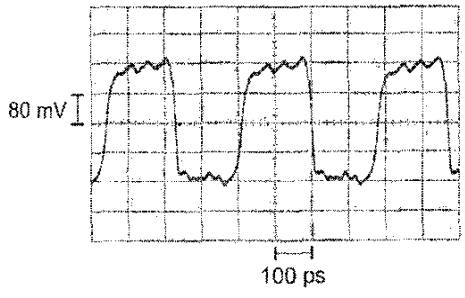

Fig. 7. Single-ended output signal of the static frequency divider (f_{in} = 86.2 GHz)

B. Dynamic Frequency Divider

The dynamic frequency divider was measured on wafer using 1.0 mm coaxial probes. Input signals with frequencies up to 50 GHz were generated by a microwave generator while millimeter-wave source modules and waveguide-to-coax adapters were used at frequencies above 50 GHz. All measurements were performed with single-ended input signals. The complementary input was not connected. The output signal of the divider was applied to a frequency counter and to a spectrum analyzer.

The dynamic frequency divider operates with a supply voltage of −5 V at a total supply current (including the output buffer) of 62 mA. Figure 8 shows the measured input sensitivity. The minimum operating frequency of the circuit is 35 GHz. The divider operates up to 110 GHz which is the highest frequency our measurement equipment provides. With a reduced supply voltage of −4.5 V the circuit still operates up to 110 GHz while consuming only 225 mW.

The single-ended output amplitude at 110 GHz input frequency is $80\,\mathrm{mV}_{pp}$ (fig. 9).

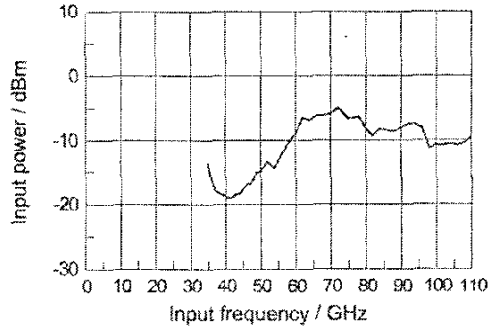

Fig. 8. Input sensitivity of the dynamic frequency divider

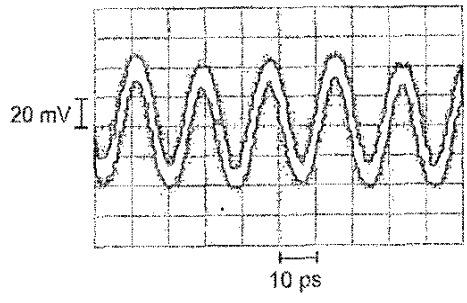

Fig. 9. Single-ended output signal of the dynamic frequency divider (f_{in} = 110 GHz)

V. Conclusions

We have presented static and dynamic frequency dividers in SiGe bipolar technology. The static divider operates up to 86.2 GHz which is the highest value published so far for silicon-based technologies.

The dynamic frequency divider is based on regenerative frequency division and operates between 35 GHz and 110 GHz (limited by the measurement setup). To the authors' knowledge this is the highest operating frequency reported so far for all IC technologies.

Table I gives a summary of the performance of the two circuits.

	Static Frequency Divider	Dynamic Frequency Divider
Divide ratio	32	2
Maximum input frequency	86:2 GHz	$\geq$ 110 GHz
Supply voltage	-5.0 V	-5.0 V
Supply current	180 mA	62 mA
Chip size	$550 \times 450\,\mu m^2$	$550 \times 450\,\mu m^2$
Technology	200 GHz f_T SiGe bipolar	

TABLE I. Frequency divider data

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